

AN ACTIVE SUBSTRATE DRIVER FOR ENABLING MIXED-VOLTAGE SOI SYSTEMS-ON-A-CHIP.

S. A. Jackson¹, B. J. Blalock¹, M. M. Mojarradi² and H. W. Li³, ¹Mississippi State University, Dept. of Electrical & Computer Engr., Box 9571, Mississippi State, MS 39762, blalock@ece.msstate.edu, ²Jet Propulsion Laboratory, 4800 Oak Grove, Pasadena, CA 91109, ³University of Idaho, Moscow, ID 83843.

Introduction: The current trend for space application systems is towards fully integrated systems-on-a-chip. To facilitate this drive, high-voltage transistors must reside on the same substrate as low-voltage transistors. These systems must also be radiation tolerant, particularly for space missions such as the Europa Lander and Titan Explorer. SOI CMOS technology offers high levels of radiation hardness. As a result, a high-voltage lateral MOSFET has been developed in a partially-depleted (PD) SOI technology [1]. Utilizing high voltages causes a parasitic transistor to have non-negligible effects on a circuit. Several circuit architectures have been used to compensate for the radiation induced threshold voltage shift of the parasitic back-channel transistor [2,3]. However, a new architecture for high-voltage systems must be employed to bias the substrate to voltage levels insuring all parasitic transistors remain off. An active substrate driver has been developed to accomplish task [4].

Circuit Description: The simplified architecture of the active substrate driver is provided in Figure 1. A $1\mu\text{A}$ current is forced through an n -type back-channel transistor (BCT). The associated top-channel channel (TCT) is connected ($V_{GS,TCT}=0\text{V}$) to remain off. The source of this BCT is biased to -5V (provided by an on-chip charge pump), insuring that its gate-source voltage is 5V greater than any other n -type BCT on the chip. Feedback will force this V_{GS} to a level allowing $1\mu\text{A}$ current to flow in this one BCT. This V_{GS} will be slightly larger than $V_{TN,BC}$, forcing the substrate voltage to be approximately 5V less than the $V_{TN,BC}$ of all other n -channel BCTs on the chip. With high levels of irradiation, both $V_{TN,BC}$ and $V_{TP,BC}$ will shift in the same direction by approximately the same amount. The active substrate driver will shift the substrate voltage by the same amount, keeping all n -type and p -type back-channel devices off.

The amplifier within Figure 1 has a low-voltage input stage (5V) and a high-voltage output stage (40V). The amplifier's output stage can provide a high-voltage output (approximately 2V to 38V). Since the amplifier directly drives the substrate and the substrate to ground capacitance can vary significantly with buried oxide thickness and die size, the stability requirements of the amplifier take into account substrate capacitance ranging from 10pF to 100pF .

Implementation and Simulation: The layout for the active substrate driver occupies a chip area of ap-

proximately $250\mu\text{m}$ by $270\mu\text{m}$ in a $0.8\mu\text{m}$ PD SOI technology. The high-voltage transistors are separated from low-voltage transistors by at least $10\mu\text{m}$. This insures thick insulating silicon dioxide between the transistors. The charge-pump has its own power supplies to reduce switching noise seen by the amplifier.

Figure 2 shows the simulation of the active-substrate driver tracking a shift in threshold voltage. BSIM3v3 device models were utilized. As V_{TH} changes, the substrate voltage follows. This simulation illustrates the fully functional active substrate driver tracking the parasitic back-channel threshold voltage shift.

References: [1] M. M. Mojarradi, *et al.*, "Power management and distribution for system on a chip for space application," (1999) *AIAA Conference*, Paper 284. [2] A. L. Caviglia, *et al.*, (1992) U. S. patent, 5,103,277. [3] J. P. Colinge, (1993) U. S. Patent 5,233,236. [4] S. A. Jackson, B. J. Blalock, M. M. Mojarradi, H. W. Li, (2000) *Proc. Southwest Symposium on Mixed-Signal Design*, 83-86.

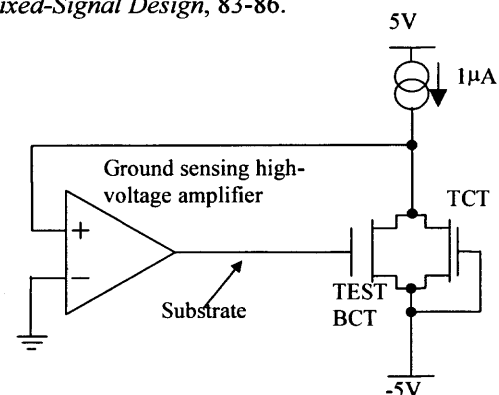


Figure 1. Active substrate driver architecture.
Figure 2. Simulated threshold voltage tracking.

